

Attorney Docket No.: 00CON161P

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In the Claims:

Claim 1 (previously presented): A method comprising steps of:

forming a layer over a transistor gate region and a field oxide region, said transistor gate region being situated over a well and said field oxide region not being situated over said well, wherein said field oxide region and said well are situated in a substrate;

forming a doping barrier above said layer over said field oxide region after said step of forming said layer;

doping said layer over said transistor gate region with a first dose of a first dopant after said step of forming said doping barrier, wherein said dose of said first dopant is a dosage greater than required to result in said layer over said transistor gate region having transistor gate electrical properties, wherein said first dopant has a first conductivity type;

removing said doping barrier after said step of doping said layer over said transistor gate region with said first dose of said first dopant;

doping said layer over said transistor gate region and said field oxide region with a second dose of a second dopant so as to form a high resistivity resistor in said layer over said field oxide region after said step of removing said doping barrier, wherein said second dopant has a second conductivity type, wherein said first dose of said first dopant is higher than said second dose of said second dopant such that said transistor gate electrical properties are unaffected by said second dose of said second dopant;

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forming a silicide blocking oxide layer over an inner portion of said layer over said field oxide region after said step of doping said layer over said transistor gate region and said field oxide region with said second dose of said second dopant;

doping an outer portion of said layer over said field oxide region with a third dopant so as to form a high-doped region in said outer portion of said layer over said field oxide region after said step of forming said silicide blocking oxide layer over said inner portion of said layer over said field oxide region, wherein said third dopant has said second conductivity type;

fabricating a contact region for said high resistivity resistor over said high-doped region in said outer portion of said layer over said field oxide region after said step of doping an outer portion of said layer over said field oxide region, wherein said contact region comprises a silicide.

Claim 2 (canceled).

Claim 3 (original): The method of claim 1 wherein said layer comprises polycrystalline silicon.

Claim 4 (previously presented): The method of claim 1 wherein said transistor gate region is a gate of an PFET.

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Claim 5 (previously presented): The method of claim 1 wherein said transistor gate region is a gate of an NFET.

Claim 6 (original): The method of claim 1 wherein said field oxide comprises silicon dioxide.

Claim 7 (original): The method of claim 1 wherein said first dopant is an N type dopant.

Claim 8 (original): The method of claim 7 wherein said N type dopant comprises phosphorous.

Claim 9 (previously presented): The method of claim 1 wherein said first dopant comprises phosphorous at a dose of approximately 6.5×10^{15} atoms per square centimeter.

Claim 10 (original): The method of claim 1 wherein said second dopant is a P type dopant.

Claim 11 (original): The method of claim 10 wherein said P type dopant comprises boron.

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Claim 12 (previously presented): The method of claim 1 wherein said second dopant comprises boron at a dose of approximately 1.0×10^{15} atoms per square centimeter.

Claims 13-25 (canceled).